AN AUDIO A/D CONVERTER USING FREQUENCY MODULATION

Publication number: WO9747090

Publication date: 1997-12-11

Inventor: DENT PAUL W

Applicant: ERICSSON GE MOBILE INC (US)

Classification:

- international: *H04R3/00; H03C3/20; H03M1/00; H03M1/60;*
H04R3/00; H03C3/00; H03M1/00; H03M1/60; (IPC1-7):
H03M1/60

- European: H03M1/60

Application number: WO1997US09038 19970603

Priority number(s): US19960657388 19960603

Also published as:

EP0972345 (A1)
US6731763 (B1)
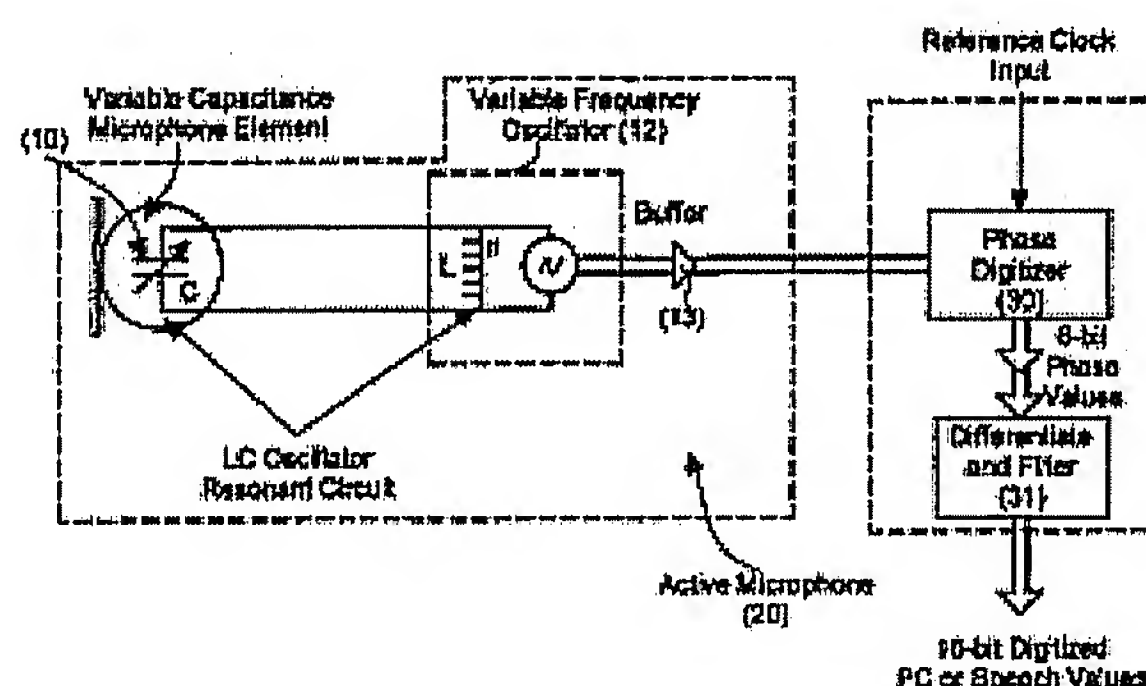US6067363 (A1)
EP0972345 (A0)
BR9709287 (A)

more >>

Cited documents:

GB2270596

Report a data error here

Abstract of **WO9747090**

According to the exemplary embodiments, a voltage or current-controlled oscillator is controlled in frequency by the signal (i.e., voltage or current) from a microphone. The frequency modulated signal is applied to a direct digital discriminator that produces a digital representation of the instantaneous frequency at the desired speech sampling rate. The digital discriminator may be formed, for example, by applying the oscillator signal to a direct phase digitizing circuit along with a reference frequency and calculating a sequence of instantaneous phases of the oscillator relative to the reference frequency. The phase sequence is then applied to a digital phase locked loop (or otherwise numerically differentiated) to generate a sequence of binary words representative of instantaneous frequency and therefore representative of the speech waveform. Since the low-level speech waveform substantially does not enter the integrated circuit except as a high-level frequency-modulated carrier, the technique is immune to noise caused by high speed random logic circuits such as microprocessors and DSPs operating on the chip.

Data supplied from the *esp@cenet* database - Worldwide

PCT

(51) International Patent Classification 6 :		(11) International Publication Number:	**WO 97/47090**
H03M 1/60	**A1**	(43) International Publication Date:	11 December 1997 (11.12.97)

(21) International Application Number: PCT/US97/09038

(22) International Filing Date: 3 June 1997 (03.06.97)

(30) Priority Data:
08/657,388   3 June 1996 (03.06.96)   US

(71) Applicant: ERICSSON INC. [US/US]; 7001 Development Drive, P.O. Box 13969, Research Triangle Park, NC 27709 (US).

(72) Inventor: DENT, Paul, W.; 637 Eagle Point Road, Pittsboro, NC 27312 (US).

(74) Agents: GRUDZIECKI, Ronald, L. et al.; Burns, Doane, Swecker & Mathis, L.L.P., P.O. Box 1404, Alexandria, VA 22313-1404 (US).

(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TR, TT, UA, UG, UZ, VN, ARIPO patent (GH, KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: AN AUDIO A/D CONVERTER USING FREQUENCY MODULATION
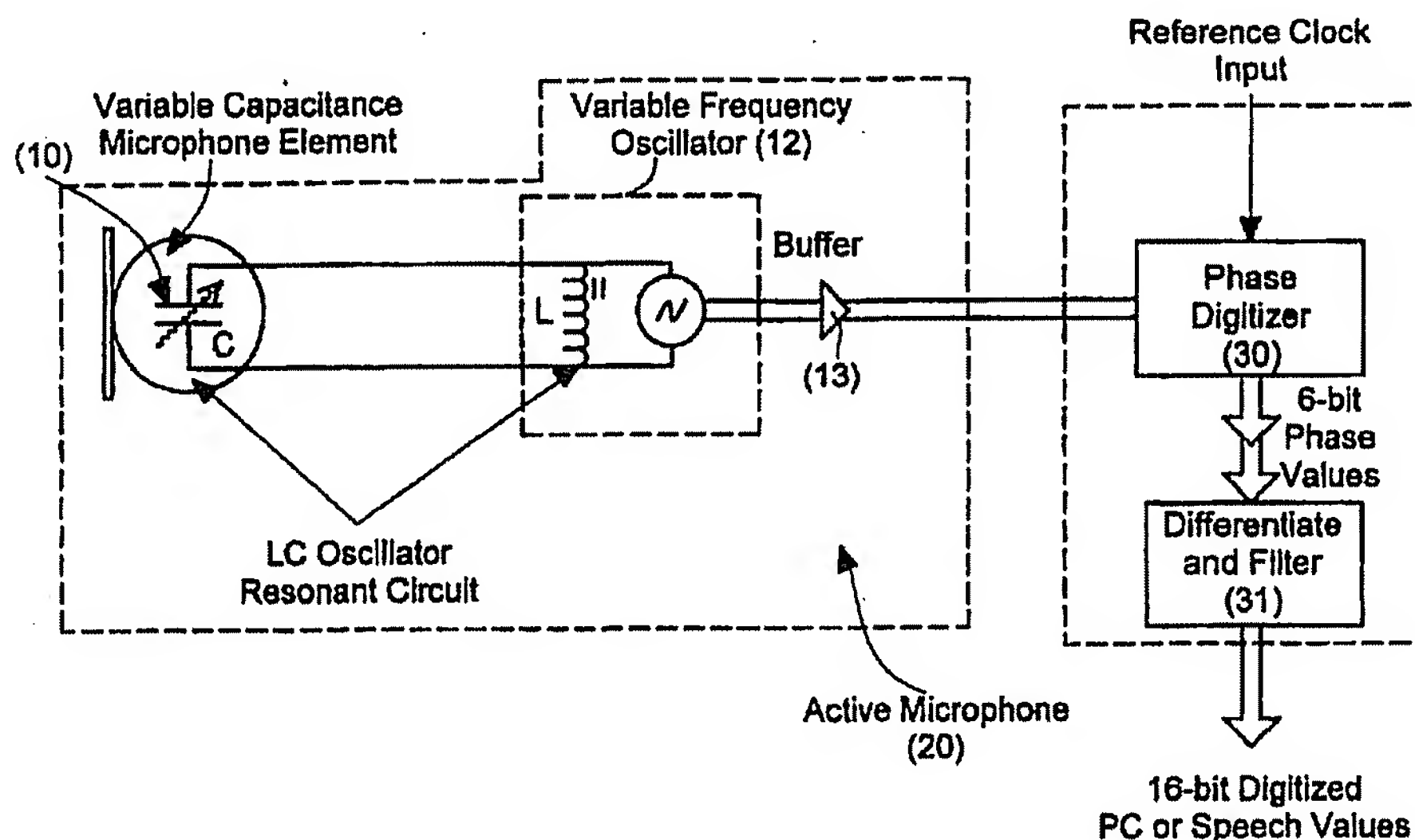
(57) Abstract

According to the exemplary embodiments, a voltage or current-controlled oscillator is controlled in frequency by the signal (i.e., voltage or current) from a microphone. The frequency modulated signal is applied to a direct digital discriminator that produces a digital representation of the instantaneous frequency at the desired speech sampling rate. The digital discriminator may be formed, for example, by applying the oscillator signal to a direct phase digitizing circuit along with a reference frequency and calculating a sequence of instantaneous phases of the oscillator relative to the reference frequency. The phase sequence is then applied to a digital phase locked loop (or otherwise numerically differentiated) to generate a sequence of binary words representative of instantaneous frequency and therefore representative of the speech waveform. Since the low-level speech waveform substantially does not enter the integrated circuit except as a high-level frequency-modulated carrier, the technique is immune to noise caused by high speed random logic circuits such as microprocessors and DSPs operating on the chip.

AN AUDIO A/D CONVERTOR USING FREQUENCY MODULATION

BACKGROUND

The present invention relates generally to reducing the cost of electronic
systems that involve voice processing, such as telephones or cellular phones, by
integrating various electronics into a single silicon chip. More particularly, the
present invention relates to analog-to-digital convertors that minimize a number of
analog components used therein and which furthermore is relatively immune to noise
pick-up from digital circuits operating in the same chip.

Many forms of conventional analog-to-digital convertors exist, for example
those known by the types of techniques used therein such as Successive
Approximation, Delta-Sigma Modulation, and Continuously Variable Slope Delta
Modulation (CVSD). The purpose of these devices is to produce a stream of numbers
representing samples of the instantaneous signal value at a desired sample rate. The
desired sampling rate is usually higher than the minimum Nyquist rate of twice the
maximum frequency of the analog signal to be numerically represented. The
drawbacks of these prior art techniques concerns the very small signal level output
from the microphone, which results in the connection between the microphone and the
analog-to-digital convertor being sensitive to noise pick-up.

SUMMARY

According to the exemplary embodiments, a variable frequency oscillator is
controlled in frequency by a variable electrical parameter in a microphone, typically a
variable capacitance. The frequency modulated signal is applied to a direct digital
discriminator that produces a digital representation of the instantaneous frequency at
the desired speech sampling rate. The digital discriminator may be formed, for
example, by applying the oscillator signal to a direct phase digitizing circuit along
with a reference frequency and calculating a sequence of instantaneous phases of the
oscillator relative to the reference frequency. The phase sequence is then applied to a
digital phase locked loop (or otherwise numerically differentiated) to generate a
sequence of binary words representative of instantaneous frequency and therefore

-2-

representative of the speech waveform. Since the low-level speech waveform substantially does not enter the integrated circuit except as a high-level frequency-modulated carrier, the technique is substantially immune to noise caused by high speed random logic circuits such as microprocessors and DSPs operating on the chip.

5   According to other exemplary embodiments of the present invention, microphone circuitry still based on the variable electrical parameter of voltage or current can be provided which is less susceptible to noise than conventional microphone circuitry. For example, conventional FET preamplifiers can be omitted according to the invention so that noise typically created by bias supplies is avoided.

10

BRIEF DESCRIPTION OF THE DRAWINGS

These features and advantages of Applicant's invention will be more readily understood by reading the following detailed description in conjunction with the drawings, in which:

15   Figure 1 is a block diagram of a digital speech processing circuit according to an exemplary embodiment of the present invention;

Figure 2 is a graph illustrating an exemplary speech frequency spectrum prior to downsampling for three exemplary quantization precisions;

Figures 3 and 4 are graphs which illustrate the quantized signal and noise

20   spectrum during quiet periods;

Figures 5 and 6 are graphs which illustrate the quantized signal and noise spectrum using a 1 KHz sine wave test;

Figure 7 is a graph which illustrates harmonic distortion for quiet period signals;

25   Figure 8 is a graph which illustrates the reduction of harmonic distortion by introduction of a deliberate frequency offset according to the present invention;

Figures 9-11 are graphs which illustrate that harmonic distortion decreases when the signal level is reduced if a deliberate frequency offset if applied according to the present invention;

30   Figure 12 is a graph which illustrates the spectrum of a noise-like test signal to which a deliberate frequency offset has been introduced;

Figure 13 is a graph illustrating a reduced signal level version of the test signal of Figure 12;

Figures 14 and 15 are graphs which illustrate residual quantizing noise residually after subtraction of the desired signal from the frequency spectrum;

5   Figures 16 and 17 are graphs which illustrate a speech pause in a signal using six-bit quantizing and residual noise therein, respectively, for a signal to which a frequency offset has been applied;

Figure 18 is a block diagram of a digital phase locked loop which can be used in systems according to the present invention;

10   Figure 19 is a graph illustrating the residual noise spectrum for an exemplary digital phase locked loop with frequency offset introduced according to the present invention;

Figure 20 is a graph which illustrates the residual noise spectrum for a phase locked loop when a frequency offset is not provided;

15   Figures 21-23 are graphs which illustrate various frequency transfer characteristics of exemplary second order phase locked loops;

Figure 24 illustrates an exemplary dynamic range specification for a typical wireless communication application;

Figure 25 is a block diagram representation of a phase locked loop which can

20   be used as a demodulator according to the present invention;

Figure 26 is a block diagram illustrating a modification of the exemplary embodiment of Figure 25 which includes mean frequency adjustment;

Figure 27 illustrates exemplary word lengths for various digital quantities used in the exemplary embodiments of Figure 26;

25   Figure 28(a) illustrates a conventional microphone circuit arrangement;

Figure 28(b) illustrates an electret microphone which controls an oscillator according to an exemplary embodiment of the present invention;

Figure 29 illustrates an exemplary source coupled multivibrator which can be used as a current controlled oscillator according to an exemplary embodiment of the

30   present invention; and

-4-

Figure 30 is a block diagram representation of a digital mixer according to an exemplary embodiment of the present invention.

DETAILED DESCRIPTION

5   U.S. Patent No. 5,084,669, which is incorporated here by reference, describes techniques for determining the instantaneous phase and frequency of a phase or frequency modulated radio signal as a series of numerical values at a desired sample rate using digital logic. U.S. Patent No. 5,220,275 to Holmqvist, which is also incorporated here by reference, describes a method of determining the instantaneous

10   phase of a signal as a numerical value computed at a desired sample rate. These digital phase/frequency determining circuits are disclosed in these patents for demodulating a modulated radio signal received by a radio receiver. The present invention employs these types of circuits in a new application for digitizing a speech signal by first converting the speech signal to a frequency modulated carrier wave and

15   then employing digital discriminator circuits to convert the modulated carrier wave signal to a train of numerical samples representative of the speech waveform.

        A first exemplary embodiment of the invention is described with the aid of Figure 1. Therein, an active microphone 20 includes a variable capacitance microphone element 10 forming part of LC resonant circuit 11 of an oscillator 12.

20   The oscillator output signal may be at a frequency of 1MHz, for example, and preferably output from active microphone 20 as a balanced signal from buffer amplifier 13. The use of balanced signal outputs whereby antiphase signals are run on parallel conductor tracks on a printed circuit board minimizes coupling to other nearby circuits, reducing the risk of causing interference and reducing interference

25   susceptibility. Acoustic speech waveforms are translated into diaphragm movements of microphone element 10 and hence into capacitance variations and then oscillator frequency variations. The speech waveform thus frequency modulates the oscillator signal and the F.M. signal is fed to a direct phase digitizer 30 such as is disclosed in the above-incorporated patents. Phase digitizer 30 compares both positive and

30   negative going transitions of the F.M. carrier signal with a reference clock and quantizes the time of occurrence of those transitions to an accuracy of, for example,

half of a clock period. The numerical result from circuit 30 is, for example, a 6-bit binary value representing instantaneous phase at an output sample rate that is a large factor higher than the final desired speech sampling rate of 8KHz. For example, the sampling rate may be 32 times higher, at 256K samples/second. The sampling rate

5   should in any case be sufficiently high that the instantaneous phase deviation of the carrier frequency from a nominal phase cannot change by more than +/-180 degrees (i.e., a half cycle) during one sample period. That is to say the sample rate should be at least twice the maximum frequency deviation from the nominal carrier frequency produced by the speech-induced diaphragm vibrations. This is desirable because a

10   greater than 180 degree phase value cannot be distinguished from a negative phase value of less than 180 degrees, and vice-versa. Preferably the phase change over one sample period should be less than +/-90 degrees to provide the greatest margin for discriminating positive from negative phase changes and avoiding the ambiguous region around +/-180 degrees.

15   The phase samples from phase digitizer 30 are fed to a numerical differentiator 31 that computes differences modulo 2Pi between successive samples. By virtue of the afore-described preferential relationship between sample rate and maximum frequency deviation, the phase difference will lie within the range +/-90 degrees. The difference will thus nominally have the same word length as the original phase

20   sample. For example, if phase is computed to 6-bit accuracy, the positive integers 0 to 31 represent angles greater than 0 and less than 180 degrees while the negative integers represent angles less than 0 and greater than -180 degrees. A phase difference nominally between +/-90 degrees is representable therefore by integers between 16 and +16, well within a 6-bit wordlength and allowing headroom for

25   greater peaks.

          The 6-bit phase differences at, for example, 256Ksamples/S are then downsampled to 8Ksamples/S by a digital low-pass filter. The first stage of such a low-pass filter can, for example, comprise computing the sum of 32 successive samples over a moving window 32-samples wide. This results in 11-bit quantities in

30   this example.

-6-

The second stage of filtering can comprise accumulating together 32 successive 11-bit moving averages once per 32-sample block to obtain 16-bit values at a sample rate of 8Ksamples/S as required. As disclosed in U.S. Patent Application Serial No. 08/120,426 filed on September 14, 1993 to Paul W. Dent which is incorporated here

5   by reference, such downsampling leads to a reduction in frequency response at the highest speech frequency of 3.4KHz, which may be compensated by resetting the accumulator before each new accumulation to a negative fraction of its previous value.

Assuming the quantizing noise on the phase differences is uniformly distributed

10   in frequency between zero and the Nyquist frequency of 128KHz, the downsampling filter reduces the quantizing noise power by the 32:1 bandwidth reduction factor, which is equivalent to 2.5 bits of precision and so the equivalent precision of this method is only 8.5 bits and not equal to the 16-bit length of the calculated values. The quantizing noise spectrum is however uniform in the phase domain, but since

15   phase is differentiated to perform frequency demodulation, the spectrum would be expected to be rising at 6dB per octave of frequency, and thus to have less noise at lower frequencies than higher frequencies. In this way, the majority of the quantizing noise power would be expected to cluster up towards half the sampling rate and the amount falling in the 0 - 3.4KHz audio band to be significantly reduced.

20   Figure 2 shows the spectrum before downsampling of the phase differences. The wanted signal modulation is a white noise signal with a spectrum extending from 200Hz to 3.4KHz representing speech, and is adjusted to produce an RMS frequency deviation of 1/3rd of a 50KHz peak deviation, chosen to be less than 1/4 of the 240KHz sample rate for the reasons explained above. This ensures that the 3-sigma

25   limits of the noise-like wanted signal are kept within the peak deviation. The spectrum of Figure 2 shows the quantizing noise outside the 3.4KHz range that will be removed by the downsampling filter, for various phase quantization accuracies in bits. Thus, the tendency for the quantizing noise spectrum to fall towards zero frequency as predicted above is confirmed. However, the quantizing noise within the

30   3.4KHz range cannot be seen in Figure 2 as this is masked by the signal spectrum. Other Figures will be discussed later that show the quantizing noise within the audio

-7-

band by subtracting the wanted signal. Figure 2 shows a band-edge quantizing noise density that is below the signal spectral density by the following amounts.

PHASE QUANTIZING	4-bit	8-bit	12-bit
BAND-EDGE N/S DENSITY	-35dB	-60dB	-85dB

These values follow the expected law of 6dB improvement per bit of quantizing accuracy, i.e., 24dB per 4-bits.

Assuming for the moment that the in-band noise falls off towards zero frequency at 6dB per octave, the total noise power can be computed by integration giving a total signal to noise power ratio 3 times (4.77dB) better than the above figures. The in-band quantizing noise can thus be expressed as an apparent noise frequency deviation in Hz RMS as follows.

PHASE QUANTIZING	4-bit	6-bit	8-bit	10-bit	12-bit
In-band noise deviation (Hz RMS)	167Hz	43Hz	10Hz	2.6Hz	0.53Hz

Speech quality is generally considered to be more related to noise in speech pauses than to noise on speech peaks. Figures 3 and 4 show the quantized signal+noise spectrum with speech modulation reduced 20 and 40dB, respectively. A tendency may be noted in these Figures for the quantizing noise at the 3.4KHz band edge to reduce with reduced signal power, which is a favorable tendency, but also there is a tendency for the spectrum to become flat, which is not so favorable. It may be shown that the greater proportion of the noise falling in the lower frequency part of the spectrum is caused by it being the signal itself which drives the phase through its quantizing levels. With lower signal excursions, the quantizing levels are crossed at a lower rate, so that the quantizing noise spectrum has more energy at low frequency.

With sine-wave signals moreover, the quantizing noise will appear at harmonics of the signal frequency, as level-crossings will occur at regularly defined points on the signal waveform. This is confirmed by Figures 5 and 6 which show an exemplary signal plus quantizing noise spectrum using a 1KHz sine-wave test signal, with 8- and 4-bit phase-quantizing, respectively. Because quantizing levels are symmetrically disposed in the phase plane, odd harmonics dominate, and the 3rd harmonic is around 66dB down on the fundamental with 8-bit quantizing and 40dB down with 4-bit quantizing. However, the relative 3rd harmonic distortion increases as the signal is reduced as shown in Figure 7, where 3rd harmonic rises to only 14dB below a 20dB reduced signal level.

These effects may be substantially alleviated by use of a deliberate carrier frequency offset such that the signal phase rotates rapidly through all the quantizing levels even in the absence of speech modulation. For example, Figure 8 shows an exemplary spectrum wherein a 20,625Hz carrier frequency offset is employed. This particular carrier frequency value is not critical and was chosen to facilitate the computation of the spectrum by giving a phase waveform that repeated in a finite number of 4096 time samples at 240Ksamples/sec. Thus, those skilled in the art will appreciate that any carrier frequency offset can be applied, however the offset should be chosen high enough so that systematic quantizing step changes occur at greater than the maximum audio frequencies. It may be seen that the third harmonic with 4-bit phase quantizing has dropped from -40dB to nearly 50dB below the fundamental. Now when the signal deviation is reduced, as shown in Figure 9, the harmonic distortion does not increase but in fact decreases, and is still in the -40dB to -50dB region with a 20dB reduced signal. Figure 10 shows that even with a 40dB reduced signal, noise and distortion products are still 25dB down. Figure 11 shows that odd harmonics appear equal to the signal when the signal power is reduced by 60dB. Figures 5 to 11 all confirm that the quantizing noise spectrum falls off towards zero frequency.

Figures 12 and 13 show the noise-like test signal using the deliberate frequency offset. Full test signal deviation is employed in Figure 12 and gives a quantizing noise spectrum with 4-bit phase quantizing that is similar to the 4-bit quantized

spectrum of Figure 2 without a frequency offset. Figure 13 however shows that, when the signal is reduced 40dB, the noise spectrum now drops about 15dB, in contrast to Figure 4, which did not use frequency offset according to the present invention. Figures 14 and 15 show the in-band quantizing noise for full signal and 40dB reduced signal respectively, having subtracted the wanted signal to unmask the residual noise. The noise spectrum is confirmed to fall off towards zero frequency and to be lower by 10 - 15dB during a -40dB speech pause (Figure 15) compared to full speech activity (Figure 14).

Figures 16 and 17 show respectively the signal+noise and residual noise spectrum during a -40dB speech pause using 6-bit phase quantizing and a deliberate frequency offset according to an exemplary embodiment of the present invention. The residual noise expressed as an in-band RMS frequency deviation is, in Figure 17, approximately 10Hz, i.e., similar to that obtained with 8-bit quantizing without frequency offset (*See* Figures 2,3).

In terms of AtoD performance, exemplary techniques according to the present invention using 6-bit phase quantizing achieve a dynamic range of 100000 units (+/-50KHz deviation or more) with a quantizing noise of 10 units RMS, i.e., -80dB relative to the whole dynamic range. A conventional AtoD convertor would require 11.5 bits precision to achieve the same performance, or 9-bits to achieve the same performance using the same oversampling factor.

An alternative method of converting phase samples to frequency samples according to the present invention is to employ a digital phase-locked loop, as described in U.S. Patent No. 5,084,669 which was incorporated above by reference. Figure 18 shows an exemplary form of digital PLL adapted for the present invention. Therein, a stream of digitized phase samples PHI1,PHI2,PHI3....PHIi...is input to a phase comparator 100. This comparator subtracts an expected phase THETAi from the actual phase PHII to obtain the error Ei between the estimate and the actual phase. The phase estimate THETAi is computed by combining a previously updated phase value delayed through delay register 101 with a previous frequency estimate delayed through delay register 105 in order to predict the new phase from the old phase by linear extrapolation using the frequency as the slope. Both the frequency and the

-10-

phase are then updated by adding a fraction BETA of the phase error to the previous frequency estimate and a fraction ALPHA of the phase error to the previous phase estimate.

ALPHA and BETA determine the characteristics of the second order digital
5   phase lock loop so constructed. It is also possible to construct higher order loops using, for example, an estimate of the rate of change of frequency which would be updated using a coefficient GAMMA.

Figure 19 shows the residual noise spectrum of the frequency estimates formed by an exemplary digital PLL having coefficients ALPHA=0.5, BETA=1/32.
10   ALPHA and BETA can, for example, be chosen to be inverse powers of two so that multiplication can be effected by a simple shift. By comparing the noise spectrum of Figure 19 with that of Figure 17, it can be seen that there is little difference within the audio range of zero to 3.4KHz, as the loop does not attenuate components in this range. A reduction in quantizing noise density at +/-15KHz is evident however as
15   the loop has some attenuation at these frequencies.

To demonstrate that the use of a deliberate frequency offset is also valuable in the context of a digital PLL FM demodulator, Figure 20 shows the residual quantizing noise from the PLL FM demodulator with the frequency offset removed. It can be seen that the quantizing noise within 0-3.4KHz is 10dB or more larger, confirming
20   that the benefit of frequency offset is independent of the type of FM demodulator used.

Figures 21, 22 and 23 are provided to show how the coefficients ALPHA and BETA can be chosen. Figures 21 to 23 give the loop attenuation from frequency in to frequency out as a function of the modulation frequency for ALPHA values of 1,0.5
25   and 0.25 and BETA values of 1 to 1/64. The loop attenuation characteristics should be substantially flat from 0 to 3.4KHz and not exhibit excessive peaking at any frequency, which is a sign of imminent instability. Another function of such a loop is that it shall track the maximum rate-of-change of frequency. This occurs when the speech modulation is the loudest. Simulations showed that the loop with
30   ALPHA=1/2, BETA=1/32 tracks the speech modulation when the RMS deviation is 16.67KHz, but fails to track a deviation of 33.33KHz RMS. It can be seen from

-11-

Figure 22 that the frequency response is approximately 3dB down at 3.4KHz with BETA=1/32. Raising the value of BETA to 1/16 with ALPHA=0.5 gives a loop which is nearly flat to 3.4KHz and the loop was confirmed to track 33.33KHz RMS deviation with these parameters. From Figure 21, the values ALPHA=0.25,

5   BETA=1/16 are also suggested, and the loop also tracks 33.333KHz deviation with those parameters. The audio SNR with 6-bit phase quantizing and 20625Hz frequency offset was computed and yielded the following figures:

RMS DEVIATION	AUDIO SNR	EQUIVALENT NOISE DEVIATION
33.33 KHz	63.8dB	22 Hz
16.67 KHz	56.5dB	25 Hz RMS
1.667 KHz	46.6dB	8.8 Hz RMS
167 Hz	25.2dB	9 Hz RMS

15

The above results show that the speech digitizing systems according to the present invention using frequency modulation possess some of the desirable characteristics of a companded method whereby the quantizing noise for small signals is less than the quantizing noise for large signals. The quantizing noise in quiet

20   periods or speech pauses is thus reduced, improving the subjective audio quality. The above results may be compared against a typical dynamic range specification for a wireless telephone application. This dynamic range specification is expressed in the diagram of Figure 24.

Therein, level 'A' indicates the RMS level of normal speech. The dynamic

25   range shall be designed to accommodate speakers talking at an average level 'B' which is 15dB higher than the normal speech level 'A'. Moreover, the speech peaks of the loudest speaker are accommodated without distortion. This is usually taken to mean in these types of specifications that the 3-sigma limit of an assumed Gaussian amplitude probability distribution shall be accommodated, or else that a +10dB crest

30   factor shall be used. This results in the level denoted by 'C' in Figure 24.

-12-

The exemplary system shall also meet a minimum signal-to-noise ratio for the quietest speaker. The quietest speaker can be characterized as speaking at a level that is 15dB below a normal speaker, namely at level 'D'. Signal-to-noise ratio is however normally defined with a sine wave test tone that has the same peak level as

5   the maximum speech level, i.e., at the peak level 'E' and not the RMS level 'D' of the quietest speaker. The Test Tone to Noise Ratio (TTNR) shall be 50dB when defined in this way. Moreover, the noise may be defined as the residual noise when the test tone signal is switched off, i.e., the noise during periods of silence. Taking into account that the RMS value of the wanted sine wave test tone energy is 3dB less

10   than its peak value, this means that the noise floor shall be 53dB below level 'E'. Comparing the noise floor level 'F', with the loudest speech peak level 'C' suggests that the total dynamic range required for a typical wireless communication application is 83dB.

By ascribing the maximum deviation that can be handled using a 240KHz

15   phase sampling rate without exceeding a phase change of Pi between samples to level C (i.e., 120KHz) then the noise floor must be 83dB below this, i.e., at 8.4Hz RMS. The above exemplary signal-to-noise simulations show a noise floor of 9Hz with 6-bit phase quantizing, which is sufficiently close to be considered meeting the specification. Nevertheless it is of interest to find ways to further reduce the

20   quantizing noise floor so as to provide some implementation margin. Exemplary techniques for reducing the noise floor could include any or all of the following: use of preemphasis, increasing the number of bits used in phase quantizing, increasing the frequency deviation and increasing the phase sampling rate. Each of these methods will be considered in turn.

25   Preemphasis is a well known technique in conventional FM radio systems for improving speech quality. With reference to the fact that most of the quantizing noise energy occurs at the top end of the audio frequency band, the frequency deviation produced by higher audio frequencies is increased at the modulator and the output of the demodulator correspondingly reduced at those frequencies, thereby attenuating the

30   dominant noise components.

-13-

Microphones are normally designed to produce a flat frequency response from sound pressure wave input to electrical signal output. Therefore to use preemphasis requires that frequency response shaping be introduced between the output of the microphone and the input to the frequency modulator. This frequency response

5   shaping produces amplification of high frequency components and therefore likely requires active circuitry. One goal of the present invention, however, is to facilitate the integration of all active circuitry on an integrated circuit chip. Therefore, on one solution can be to design the acoustic (i.e., mechanical) components of the microphone such as its diaphragm and surrounding cavities to effect an acoustic pre-

10   emphasis. Alternatively, preemphasis circuit would preferably be integrated on a chip with external connections to the microphone. The microphone signals would thus enter the chip at a low level before amplification at which point they would be susceptible to noise pick-up. This form of preemphasis is not, therefore, the preferred solution although those skilled in the art will recognize when design

15   tradeoffs will make this an acceptable solution.

A preferred form of preemphasis would be to use a microphone with a naturally rising frequency response that produces larger electrical inputs for the same sound pressure vibration level at higher frequencies. Such specially tailored microphones may not, however, be generally available, so the other methods

20   described of obtaining improved voice quality (e.g., using one more bit of phase precision) can be employed in conjunction with any available microphone.

One method to improve voice quality is to increase the number of bits used to represent quantized phase. Each extra bit of phase quantizing accuracy provides a 6dB improvement of audio quality. Increasing phase quantizing accuracy equates to

25   timing transitions of the FM carrier signal to a finer time accuracy. This can be done by utilizing a higher clock frequency as the reference for the phase digitizer, or by timing transitions to a fraction of a clock cycle. For example, a sawtooth clock waveform can be generated with a linear ramp-up with a repetitive reset-to-zero. The ramp can be sampled upon the occurrence of transitions of the FM carrier signal to

30   determine its amplitude, thereby quantizing the transition time to a fraction of a clock cycle. Other related methods can include the generation of sine and cosine clock

waveforms which are sampled upon occurrence of a transition, the fractional phase value then being given by the arctangent of the sine/cosine sample ratio. These methods involve analog circuit concepts which are not especially desirable for integration onto a digital integrated circuit. A method more suitable for integration is

5   to compute an average phase over more than one transition occurring between phase sampling instants. For example, if phase is to be sampled at 240Ksamples/S and the FM carrier frequency is nominally 1MHz, there will be at least three positive-going transitions and at least three negative going transitions of the carrier within each 240KHz period. Both negative transitions and positive transitions can be used if the

10   phase samples produced by the former are corrected for the 180 degree phase difference between half-cycles. Care should be exercised when averaging angle measurements, as the correct average of -179 and +179 degrees is 180 degrees and not zero. The theoretically best method to average angles is to average their cosines and their sines separately and to calculate the ARCTAN of the result. This technique

15   is known as circular averaging.

       The aforementioned digital phase locked loop (PLL) provides a simpler practical method for averaging phase measurements from a large number of signal transitions. Furthermore, the phase digitizer (not shown) preceding the digital PLL of Figure 18 may be eliminated, and the phase digitization performed by the PLL itself.

20   This reduction is possible because the current application of the PLL for inventive digitization of an audio signal involves digital FM demodulation in the absence of radio noise.

       An exemplary PLL system is shown in Figure 25. The FM input signal is applied to transition detector 110. When the input signal transitions from a previous

25   logic '0' level which has been stored in flip-flop 111 to a logic '1' level, then the Q output of flip-flop 111 will be a '1' and the inputs of two-input NAND gate 112 will be fulfilled, applying a logic '0' to the D input of flip-flop 113. This input will be registered in flip-flop 113 upon occurrence of the reference clock pulse resulting in a rising edge on the Q output of 113 and a falling edge on the Q output. A binary logic

30   '1' on the Q output operates gate 127 to allow the contents of phase accumulator 120 to appear on the output of gate 127 as long as the control input is a logic '1'. This

-15-

value is multiplied by ALPHA in multiplier 125 and subtracted from the phase value
PHI received from accumulator 120 in subtractor 122. This occurs for a single
reference clock cycle, because after the FM signal input's transition has passed, the Q
output of flip-flop 113 will return to logic '0' causing gate 127 to resume outputting
5 the value zero. The value ALPHA.E will thus be added to the phase accumulator 120
only once, while the frequency value ω gets added at every reference clock pulse.
While gate 127 is passing the phase accumulator value, it is also multiplied by BETA
in multiplier 126 and subtracted from the previous value of ω in subtractor 124. The
new value is then registered in integrator register 123 on the rising edge of the Q
10 output of flip-flop 113, coincident with gate 127 being returned to the zero output
condition. The decrement BETA.E to the previous value of ω is thus permanent.
The modified value of ω permanently affects the rate at which phase accumulator 120
increments, i.e., it affects the phase derivative, while the value ALPHA.E affects the
phase only once, permanently affecting the phase value but not its derivative. In this
15 way the coefficients ALPHA and BETA may be chosen to form a second order digital
phase lock loop with desired characteristics as before. ALPHA and BETA are
preferably chosen to be inverse powers of two so that the multiplication reduces to a
shift. The values of ALPHA and BETA are analogous to those of the previous
discussion on digital PLL design, except that the value of BETA is scaled down
20 because the phase derivative value ω is added to the phase accumulator 120 many
times between each iteration. The number of additions is equal to the number of
reference clock pulse periods in a nominal period of the FM input signal. For
example, suppose the FM input signal frequency is 620KHz and the reference clock is
19.2MHz. On average, the value ω is added to the phase accumulator 19200/620 =
25 31 times approximately per cycle of the FM input. The value of BETA thus should
be about 1/32 of the values indicated in Figures 21-23 for this exemplary PLL.
Moreover the loop frequency response characteristics will exhibit a wider bandwidth
in proportion to the increased update frequency, which is now equal to the FM input
frequency, for example 620KHz instead of 240KHz. Thus lower values of ALPHA
30 and BETA should be used to maintain similar loop frequency responses. Since the
frequency value ω will be sampled by a lower frequency sampling clock using sampler

-16-

130, it is desirable that the loop frequency characteristics attenuate frequencies above half the final sampling rate in order to avoid the aliasing phenomenon. Figure 21 can be used to find appropriate values of ALPHA and BETA as follows.

The loop update rate (e.g., 620KHz) is 620/240 times that used to produce
5   Figure 21, so the horizontal frequency scale is scaled accordingly. The values ALPHA=0.25, BETA=1/32 produced a bandwidth flat to about 4KHz before, and thus would be flat to 4KHz x 620/240 = 10.33KHz with the higher update rate. The loop previously exhibited 30dB of attenuation at 45KHz approximately. Thus 30dB of attenuation will occur at 45KHz x 620/240, which is less than half the 240KHz
10   sampling rate envisaged for sampler 130. The loop should thus provide adequate attenuation of aliasing components without extra digital filtering prior to sampling. The exemplary values of ALPHA and BETA suggested for the arrangement of Figure 25 are thus ALPHA=0.25, BETA=1/1024, the 32:1 reduction of BETA being for the reasons discussed above.

15   The value of ω held in flip-flop 123 of Figure 25 represents the input signal carrier frequency ω_0 plus the instantaneous frequency deviation $d\omega$ due to the audio modulation. Only the latter is of interest so the mean frequency ϖ_0 should be removed before sampling. In Figure 25 this is accomplished by subtractor 131. The mean frequency subtracted can be computed by later digital signal processing and fed
20   back, so no specific circuitry is shown in Figure 25 for computing the mean frequency.

In other exemplary embodiments, it may be desirable that some provision be made to set the initial contents of flip-flop 123 to the expected mean frequency in order to avoid delay in initial acquisition of phase lock. This can be accomplished at
25   the same time as subtracting the mean frequency by the re-arrangement of Figure 26. In Figure 26, the frequency flip-flop 123 holds the deviation of frequency $d\omega$ from the mean. Instead of the subtractor 131 of Figure 25, adder 132 of Figure 26 is provided. The adder 132 adds the mean frequency ϖ_0 to obtain the increment rate $\omega = \varpi_0 + d\omega$ of the phase accumulator. This mean frequency is envisaged to be set by
30   feedback from further processing, and thus accomplishes both the initial frequency

-17-

setting function and the elimination of the mean frequency from the sampled output of sampler 130.

Figure 27 illustrates exemplary word lengths of the various digital quantities in Figure 26. The phase accumulator 120 is shown as the 21-bit register A, along with the phase and frequency significance of its bits. The frequency significance applies when the indicated bit is added at a 19.2MHz rate. For example, if a most significant 11, is repetitively added, the phase accumulator will execute the sequence 10000 ..., 00000..., 10000..., etc., which represents the phase sequence 0,Pi,0,Pi....This produces a complete cycle every two reference clock periods, that is 9.6 Megacycles per second. Each successive bit has half the frequency significance and the least bit has approximately 9Hz significance. (9.6MHz/2**20)

The increment ω_0 required to produce a nominal frequency of 620.625KHz is shown in register B of Figure 27. The most significant four bits of the increment are zero as is the least significant bit, thus 16-bits are sufficient to define ω_0. The frequency deviation $d\omega$ around ω_0 is represented by register C. If the frequency deviation is within +/-150KHz it can be represented by a 16-bit value. The most significant bit (i.e., the 150KHz accumulator bit) is regarded as the sign and is sign extended for addition to phase accumulator 120. The instantaneous frequency deviation value $d\omega$ is updated by subtracting 1/1024 of the phase accumulator's value at the moment the input signal undergoes a positive transition. Register D shows the accumulator value shifted back by 10 binary places representing division by 1024. The twelve remaining bits are sign extended to 16 bits in Register D for addition to the 16-bit dw value C. Finally, register E shows the accumulator multiplied by ALPHA (e.g., 0.25) which is a two-bit left-shift.

In Figure 26, the accumulator phase value is tested with every input signal transition from low to high, at a rate of greater than 470KHz so that the frequency deviation is never more than 150KHz. If the phase change between samples shall at the absolute maximum never be greater than +/-Pi, a peak frequency deviation of 235KHz can be used. In fact, according to this exemplary embodiment, the frequency can deviate no more than +/-150KHz, which is still an increase on the exemplary system of Figures 2-24 which restricted the frequency deviation to about 100KHz.

-18-

The normal audio deviation may thus be increased by approximately 3dB compared with the values previously considered, giving a dynamic range improvement of 3dB. On the other hand, input signal transitions were previously envisaged to be quantized to a half cycle of the 19.2MHz reference clock giving 6-bit phase quantizing.

5   Transitions are quantized in the systems of Figures 25 and 26 to one cycle of the reference clock, reducing the equivalent phase quantizing accuracy to 5-bits, a loss of 6dB. However, this is more than made up by the increase in sampling rate from 240KHz to 600KHz approx, as the quantizing noise power in the 3.4KHz audio range reduces with the cube of the sampling rate (9dB for 2:1). The arrangement of Figures
10   25-27 is thus expected to show at least a net 6dB reduction of quantizing noise after downsampling the frequency output words to 8K samples/second.

       Methods for converting an acoustic pressure wave to a frequency or phase modulated electrical signal can include the use of a capacitor microphone, which forms part of the resonant circuit of an oscillator; a variable inductance microphone
15   forming part of an oscillator circuit; air electret or piezoelectric crystal microphone connected to one or more variable capacitance diodes which form part of an oscillator circuit, or any microphone producing a voltage or current signal that controls a voltage or current-controlled oscillator. Figure 28(a) illustrates a conventional microphone arrangement. The conventional arrangement includes microphone 210
20   containing piezoelectric transducer 208, high value resistor 207 and FET pre-amplifier 206. The FET preamplifier commonly has an open collector output which is used both to apply bias to the FET and to obtain the audio output, the microphone thereby remaining a two-terminal component. Bias is applied from low-noise bias voltage source 201 through resistor 205 across which the current flow through the FET
25   develops the audio signal. The DC voltage level on the output is arbitrary and is removed by blocking capacitor 204 before further amplification in microphone amplifier 202. One disadvantage of this conventional arrangement is the need for the exceptionally low-noise bias supply 201. Typically, the normal RMS voice signal from the microphone corresponding to level A of Figure 24 is 5mV RMS. The noise
30   floor is required to be 58dB below this level, that is 6μV. The conventional circuit of Figure 28(a) is, however, very susceptible to noise from the bias supply as well as to

noise pickup on the signal from resistor 205 through capacitor 204 and resistor 203 to microphone amplifier 202.

An exemplary microphone arrangement which overcomes these disadvantages according to the present invention is shown in Figure 28(b). Therein, microphone

5   220 now incorporates piezoelectric element 208 and resistor 207 as before but lacks FET pre-amplifier 206. No bias supply current is therefore needed. Instead the piezoelectric element (electret) 208 output voltage varies the capacitance of varactor diodes 211 and 212 which, with inductor 213, form the resonant circuit for oscillator 230. The oscillator is preferably a relatively low-level oscillator that does not apply

10   enough AC voltage swing to varactor diodes 211 and 212 that they might be driven into forward conduction. It is preferable to operate varactor diodes 211 and 212 with zero reverse bias voltage to avoid the need to generate a low-noise bias voltage, and also in order to maximize the frequency-modulation sensitivity of the oscillator. A ground line from a center-tap on inductor 213 (illustrated by a dotted line in Figure

15   28(b)) is suggested to ensure that no low-frequency (audio) noise pickup can occur on the lines between varactors 211 and 212 and inductor 213. The low-level oscillation produced by oscillator 230 may nevertheless be 100mV or more as the varactor diodes will not be driven into forward conduction until 300-400mV is reached. The oscillator signal is thus 20 times higher than the microphone signal of the conventional

20   microphone circuit arrangement of Figure 28(a), and furthermore is a high frequency FM signal that is relatively immune to interference pickup. In this way the inventive system provides both circuit simplification by elimination of the bias supply 201 and microphone amplifier 202 as well as greatly reduced susceptibility to noise pickup.

Alternatively, a circuit using a current-controlled oscillator can be used, an

25   example of which is shown in Figure 29. A known form of current controlled oscillator is the emitter-coupled multivibrator, or its FET equivalent, the source-coupled multivibrator, which is shown in Figure 29. Microphone 210 now includes the electret element 208 and two identical FET transconductance amplifiers 206a and 206b which convert the electret audio voltage to a pair of audio current sources of

30   magnitude I. These currents form the tail currents of N-type FETs 241 and 242 which are cross-coupled drain-to-gate and source-coupled by timing capacitor C 240.

-20-

It can be shown that the circuit will oscillate with approximately the source waveforms indicated and with a frequency that is proportional to the current I. Providing that FETs 206a and 206b are good current sources, the audio current I and therefore the frequency modulation will not be strongly dependent on the supply

5   voltage Vcc, thus a measure of immunity to supply voltage noise is obtained.

It may be desirable, in order to obtain a sufficiently high frequency deviation with any of the above described methods, to use a frequency modulated oscillator of a high frequency which is then mixed down to the desired 620KHz range. Producing a peak deviation of, for example, +/-150KHz of a 620KHz oscillator could otherwise

10   be difficult, as this is a high percentage change. On the other hand, producing a +/-150KHz peak deviation of a 18.6MHz oscillator, which is then mixed down to the 600KHz range against a 19.2MHz reference oscillator is more straightforward. A suitable mixing arrangement can be formed using digital logic components as shown in Figure 30.

15   Therein, the FM input signal at nominally 18.6MHz is applied to the D input of edge triggered flip-flops 400 and 401. Flip-flop 400 is clocked by the 19.2MHz reference clock and flip-flop 401 by the inverted clock. The flip-flops produce square-wave outputs at the 600KHz difference frequency that are relatively inverted. The relative inversion is rectified by using the Q output of flip-flop 400 and the $\overline{Q}$

20   output of flip-flop 401. Moreover, the 600KHz output of flip-flop 400 has transitions that are synchronized to the 19.2MHz clock rising edges while the output of flip-flop 401 is synchronized to the falling edges. Between the two, transitions of the 600KHz difference frequency are thus preserved to a half cycle accuracy of the reference clock, which is used to obtain 6-bit phase quantizing.

25   The 19.2MHz clock also drives reference divide-by-32 circuit 402. The output of circuit 402 increments on rising edges of the clock and is stable during the falling edge of the clock. The output of circuit 402 is also retimed to falling edges of the clock by latch 405. Thus the count sequence produced by circuit 402 and latch 405 is, for example:

30   Circuit 402:   ...25   26   27   28   29   30   31   0   1   2 .....

Latch 405: 25   26   27   28   29   30   31   0   1   2 ....

-21-

Now depending on the transition timing of the 18.6MHz FM input signal, a rising edge on the 600KHz Q output of flip-flop 400 may occur one half cycle of the reference clock before a rising edge on the Q output of flip-flop 401 or vice versa. If the former occurs first, for example, at count 27 out of counter 402, the contents of

5   latch 405 at that time will be 26, which number will be latched into latch 404. Then the output of flip-flop 401 will occur at count 27 of latch 405, at which point circuit 402 still contains 27, which number will become latched into latch 403. The sum of latches 403 and 404 produced by adder 406 will then be the 6-bit number 26+27 = 53.

10   If, on the other hand, the transition on the Q output of flip-flop 401 occurs on the clock half cycle before the Q output of 400 at the value 26 out of latch 405, then circuit 402 at that time contains the value 26, which will thus be latched in latch 403. Then, when the transition on the Q output of flip-flop 400 occurs at count 27 of circuit 402, latch 405 still contains 26, which value becomes latched in latch 404.

15   The sum produced by adder 406 in this instance is 26 + 26 = 52, reflecting the occurrence of the 18.6MHz input transition one half clock cycle earlier. In this way the sum output of adder 406 represents the signal phase to a timing accuracy of half a reference clock cycle. The 6-bit phase sequences are applied to a digital PLL 407 according to Figure 18 along with a clock derived from the Q output of flip-flop 401

20   thus ensuring that phase values are only used long after the output of adder 406 has become stable. The ALPHA,BETA values of PLL 407 are chosen to provide the desired frequency response with the clock rate of 600KHz, as previously described. The increased clock rate of 600KHz compared to the value of 240KHz that was analyzed in detail above provides at least 9dB reduction of quantizing noise. The

25   frequency estimates calculated and filtered by the PLL are then downsampled to 240KHz by the output of divide-by-80 circuit 408. This is clocked by the rising edges of the reference clock while the PLL 407 updates its values synchronously with the falling edges, thus ensuring that downsampling occurs after updated frequency values have become stable. The 240Ksamples/S frequency values may then be further

30   downsampled to 8KHz using known downsampling filter techniques.

A number of variations of the invention have been disclosed from which further derivatives may be constructed by persons skilled in the art, while still adhering to the scope and spirit of the invention as described by the following claims.

-23-

I claim:

1. A method of digitizing an audio signal comprising the steps of :

frequency modulating an oscillator with said audio signal;

applying said frequency-modulated oscillator's signal to a digital

5   frequency discriminator that computes a sequence of instantaneous frequency values;
and

using said instantaneous frequency values as said digitized audio signal.

2. A method of digitizing an audio signal to produce a sequence of

10   representative numerical values at desired sampling instants comprising the steps of:

frequency modulating an oscillator with said audio signal;

combining said frequency-modulated oscillator's signal with a reference

frequency clock to produce a sequence of instantaneous phase values of said oscillator

signal; and

15   numerically estimating a rate of change of said instantaneous phase

values at said desired sampling instants and using said estimated rate of change values

as said representative numerical values.

3. A method of digitizing an audio signal according to claim 1 in which

20   said digital frequency discriminator is a digital phase lock loop.

4. A method of digitizing an audio signal according to claim 2 in which

said estimation of rate of change of phase is performed using a digital phase lock

loop.

25

5. A method of digitizing an audio signal according to claim 2 in which

said estimation of rate of change of phase is performed by differencing successive

phase values.

30   6. A method of producing a sampled digital representation of an acoustic

pressure wave comprising the steps of:

-24-

converting said acoustic pressure wave to corresponding variations in electrical capacitance;

using said variations in electrical capacitance to produce corresponding variations in a frequency of an electrical oscillator's signal;

5   applying said frequency-modulated oscillator's signal to a digital frequency discriminator that computes a sequence of instantaneous frequency values; and

using said instantaneous frequency values as said digitized audio signal.

10   7.   A method of producing a sampled digital representation of an acoustic pressure wave comprising the steps of :

converting said acoustic pressure wave to corresponding variations in electrical capacitance;

using said variations in electrical capacitance to produce corresponding
15   variations in a frequency of an electrical oscillator's signal;

combining said frequency-modulated oscillator's signal with a reference frequency clock to produce a sequence of instantaneous phase values of said oscillator signal; and

numerically estimating a rate of change of said instantaneous phase
20   values at said desired sampling instants and using said estimated rate of change values as said representative numerical values.

8.   A method of digitizing an audio signal according to claim 7 in which said digital frequency discriminator is a digital phase lock loop.

25

9.   A method of digitizing an audio signal according to claim 6 in which said estimation of rate of change of phase is performed using a digital phase lock loop.

-25-

10.   A method of digitizing an audio signal according to claim 6 in which said estimation of rate of change of phase is performed by differencing successive phase values.

5   11.   A method according to claim 6 in which said variations in electrical capacitance are produced using a capacitance microphone.

12.   A method according to claim 7 in which said variations in electrical capacitance are produced using a capacitance microphone.

10

13.   A method according to claim 6 in which said variations in electrical capacitance are produced using a piezoelectric microphone and a variable capacitance diode.

15   14.   A method according to claim 7 in which said variations in electrical capacitance are produced using a piezoelectric microphone and a variable capacitance diode.

15.   A method according to claim 1 in which said oscillator's center
20   frequency is offset from said digital discriminator's center frequency by more than a highest audio frequency.

16.   A method according to claim 2 in which said oscillator's center frequency is offset from a submultiple of said reference clock frequency by more than
25   a highest audio frequency.

17.   An analog-to-digital convertor for producing a sequence of numerical sample values representative of a signal waveform comprising:

        oscillator means to produce a high frequency signal;

-26-

frequency/phase modulating means to change are of the frequency and phase angle of said high frequency signal in correspondence with said signal waveform;

digital frequency discriminator means to determine numerical values for

5   said oscillator's instantaneous signal frequency at determined sampling instants;

digital frequency discriminator means to determine numerical values for said oscillator's instantaneous signal frequency at determined sampling instants; and

output means to output said numerical values as said representative numerical sample values.

10

18.   An analog-to-digital convertor according to claim 17 further comprising:

downsampling means for filtering said instantaneous numerical frequency values to produce filtered samples at a reduced sample rate.

15

19.   An analog-to-digital convertor for producing a sequence of numerical sample values at a first sample rate representative of a signal waveform comprising:

oscillator means to produce a high frequency signal;

frequency/phase modulating means to change the frequency or phase

20   angle of said high frequency signal in correspondence with said signal waveform;

direct phase digitizing means for combining said oscillator signal with a reference frequency clock signal in order to generate numerical values representative of instantaneous phase at a second sampling rate; and

processing means to process said phase samples at said second sampling

25   rate in order to generate said signal waveform representative samples at said first sampling rate.

20.   An analog-to-digital convertor according to claim 19 in which said processing means reduces quantizing noise by digital low-pass filtering.

30

-27-

21.   An analog-to-digital convertor according to claim 19 in which said processing means includes a digital phase lock loop.

22.   A microphone circuit with immunity to electrical noise pickup for producing a numerical sample stream representative of a sound pressure wave comprising:

transducer means for converting sound pressure wave variations to corresponding variations in an electrical parameter;

oscillator means for producing an oscillator signal having a frequency dependent on said electrical parameter;

digital frequency discriminator means to determine numerical values for said oscillator's instantaneous signal frequency at determined sampling instants; and

output means to output said numerical values as said representative numerical sample stream.

23.   A microphone circuit with immunity to electrical noise pickup for producing a numerical sample stream at a first sample rate representative of a sound pressure wave comprising:

transducer means for converting sound pressure wave variations to corresponding variations in an electrical parameter;

oscillator means for producing an oscillator signal having a frequency dependent on said electrical parameter;

direct phase digitizing means for combining said oscillator signal with a reference frequency clock signal in order to generate numerical values representative of instantaneous phase at a second sampling rate; and

processing means to process said numerical values at said second sampling rate in order to generate said numerical sample stream at said first sampling rate.

24.   A microphone circuit according to claim 23 in which said processing means reduces quantizing noise by digital low-pass filtering.

25.   A microphone circuit according to claim 23 in which said processing means includes a digital phase lock loop.

26.   A microphone circuit according to claim 22 in which said transducer means is a piezoelectric transducer.

27.   A microphone circuit according to claim 22 in which said electrical parameter is capacitance.

28.   A microphone circuit according to claim 23 in which said transducer means is a piezoelectric transducer.

29.   A microphone circuit according to claim 23 in which said electrical parameter is capacitance.

30.   A microphone with immunity to electrical noise pick-up comprising:
       a ground terminal and a signal terminal;
       a piezoelectric transducer for converting sound pressure waves to a corresponding electrical voltage signal between a first and a second terminal, said second terminal being connected to said ground terminal;
       an electrical resistor connected between said transducer's first and second terminal; and
       a varactor diode having one terminal connected to said transducer's first terminal and its other terminal connected to said signal terminal.

31.   A microphone with immunity to electrical noise pick-up comprising:
       a ground terminal and first and second signal terminals;
       a piezoelectric transducer for converting sound pressure waves to a corresponding electrical voltage signal between a first and a second terminal, said second terminal being connected to said ground terminal;

-29-

an electrical resistor connected between said transducer's first and second terminal;

a first varactor diode having an anode connected to said transducer's first terminal and a cathode connected to said first signal terminal; and

5   a second varactor diode having an anode connected to said transducer's first terminal and a cathode connected to said second signal terminal.

32.   A microphone according to claim 31 further comprising:

an inductance connected to said first and second signal terminals and

10   forming part of an oscillator circuit.

33.   A microphone with immunity to electrical noise pick-up comprising:

a ground terminal and first and second output terminals;

a piezoelectric transducer for converting sound pressure waves to a

15   corresponding electrical voltage signal between a first and a second terminal, said second terminal being connected to said ground terminal;

an electrical resistor connected between said transducer's first and second terminal;

a first field effect transistor having a gate electrode connected to said

20   transducer's first terminal, a source electrode connected to said ground terminal and a drain electrode connected to said first output terminal; and

a second field effect transistor having a gate electrode connected to said transducer's first terminal, a source electrode connected to said ground terminal and a drain electrode connected to said second output terminal.

25

34.   A microphone according to claim 33 further comprising:

current controlled oscillator means connected to said first and second output terminals to produce a frequency modulated oscillation signal.

35.   A microphone circuit with immunity to electrical noise pickup for producing a numerical sample stream at a first sample rate representative of a sound pressure wave comprising:

transducer means for converting sound pressure wave variations to

5   corresponding variations in an electrical parameter;

oscillator means for producing an oscillator signal having a frequency dependent on said electrical parameter;

digital mixing means for combining said oscillator signal with a reference frequency clock signal to produce at least one difference frequency signal;

10   direct phase digitizing means for combining said at least one difference frequency signal with said reference frequency clock signal to generate numerical values representative of instantaneous phase at a second sampling rate; and

processing means to process said numerical values at said second sampling rate to generate said numerical sample stream at said first sampling rate.

FIG. 1

FIG. 2

FIG. 3

FIG. 4

FIGURE 5

FIG. 6

1 KHz Test Tone Modulation

Peak Deviation = $\dfrac{50\ KHz}{3}$

-1 KHz　+1 KHz

= 4 Bit Phase Quantizing

+15 KHz

0

-15 KHz

dbs

0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
-110
-120
-130
-140
-150
-160

FIG. 7

= 4 Bit
Phase
Quantizing

$$\text{Peak Deviation} = \frac{50 \text{ KHz}}{30}$$

-1 KHz   +1 KHz

+15 KHz

0

-15 KHz

dbs

0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
-110
-120
-130
-140
-150
-160

FIG. 8

DC (Frequency Offset = 20625 Hz)

$\left(\text{Peak Deviation} = \dfrac{50\ \text{KHz}}{3}\right)$

= 4 Bit Phase Quantizing

-1 KHz   +1 KHz

+15 KHz

0

-15 KHz

dbs

0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
-110
-120
-130
-140
-150
-160

FIG. 9

DC (Frequency Offset = 20625 Hz)

(Peak Deviation = 1667 Hz)

$$\frac{50 \text{ KHz}}{30}$$

-1 KHz +1 KHz

= 4 Bit
Phase
Quantizing

+15 KHz

0

-15 KHz

dbs

0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
-110
-120
-130
-140
-150
-160

FIG. 10

DC (Frequency Offset = 20625 Hz)

$$\text{Peak Deviation} = \frac{50\ KHz}{300}$$

-1 KHz   +1 KHz

= 4 Bit
Phase
Quantizing

+15 KHz

0

-15 KHz

dbs

0 -10 -20 -30 -40 -50 -60 -70 -80 -90 -100 -110 -120 -130 -140 -150 -160

FIG. 11

DC (Frequency Offset = 20625 Hz)

$$\left(\text{Peak Deviation} = \frac{50 \text{ KHz}}{3000} \right)$$

-1 KHz +1 KHz

+15 KHz

0

-15 KHz

0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
-110
-120
-130
-140
-150
-160

dbs

FIG. 12

FIG. 13

DC (Frequency Offset = 20625 Hz)

RMS Deviation 167 Hz $\left(\frac{50 \text{ KHz}}{300} \right)$

= 4 Bit Phase Quantizing

FIGURE 14

FIG. 15

= 4 Bit Quantizing of Phase

RMS Frequency Deviation = 16667 Hz $\left(\dfrac{50\ KHz}{300}\right)$

DC (Offset Frequency = 20625 Hz)

+15 KHz

-15 KHz

dbs

0 -10 -20 -30 -40 -50 -60 -70 -80 -90 -100 -110 -120 -130 -140 -150 -160
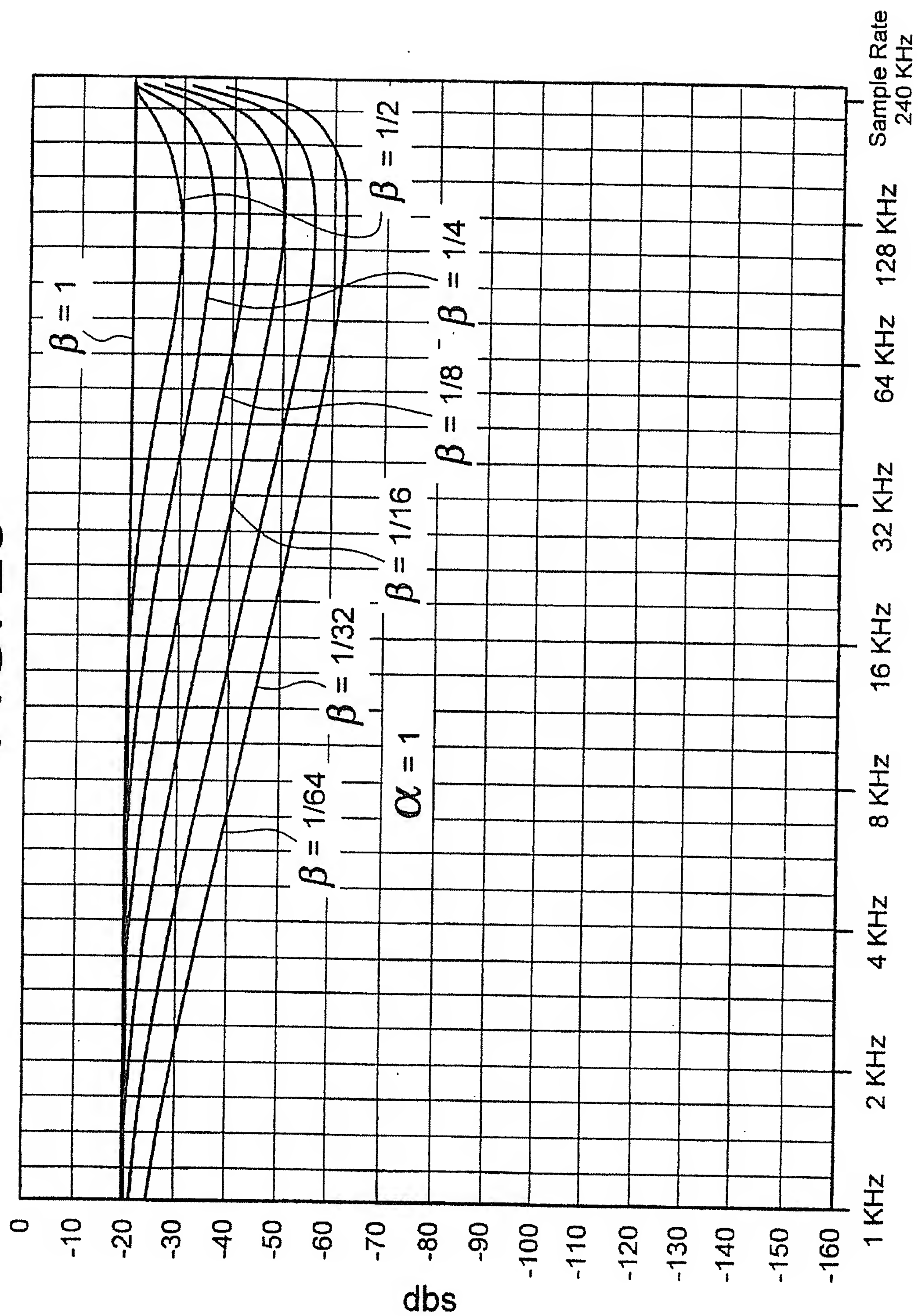
FIGURE 16

FIGURE 17

FIG. 18

FIGURE 19
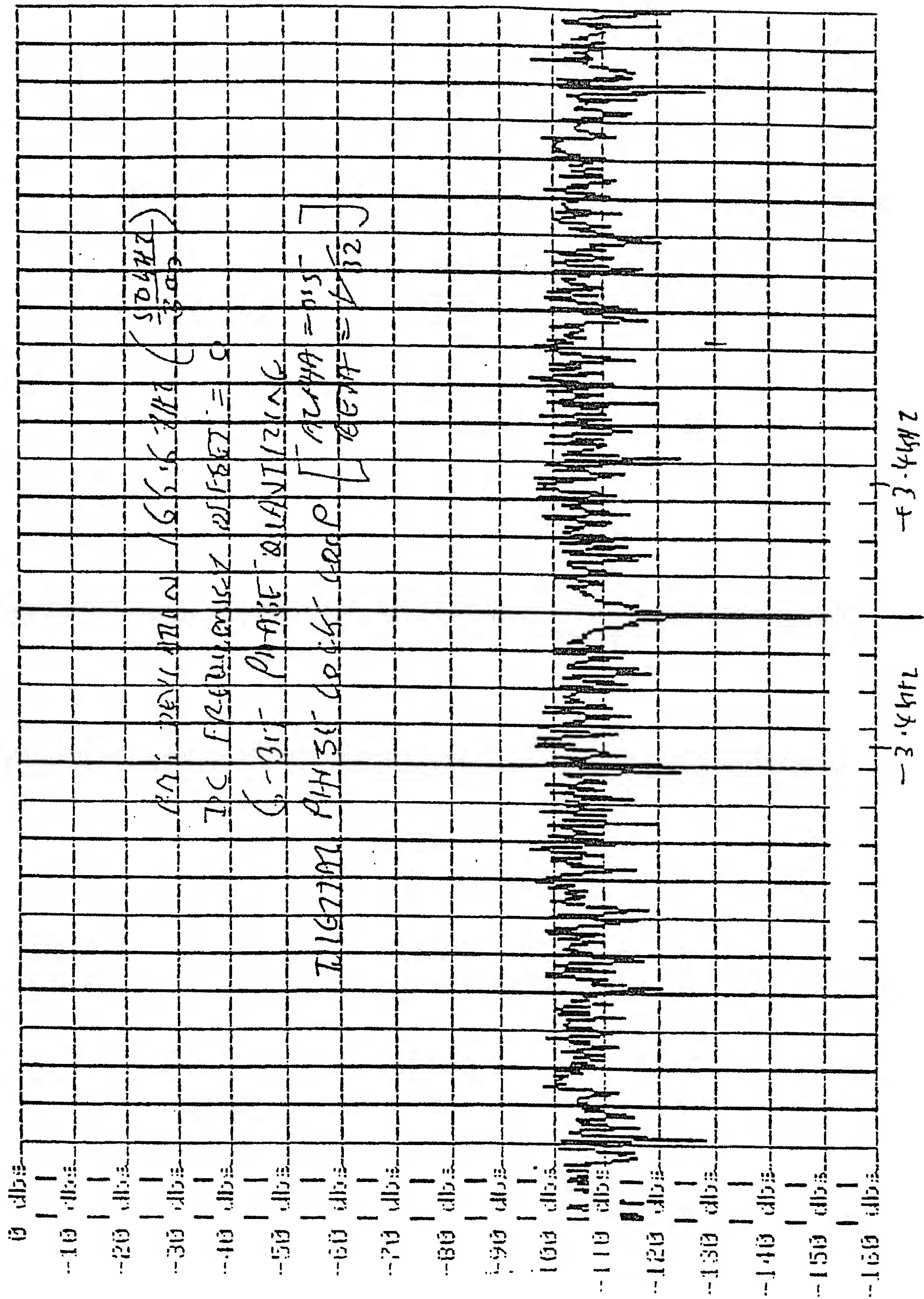
FIGURE 20

FIG. 21

FIGURE 22

FIG. 23

FIG. 24

FIG. 25

FIG. 26

A — FREQUENCY SIGNIFICANCE WITH 19.2 MHz INCREMENT RATE / 22-BIT PHASE ACCUMULATOR (120)

4.5 Hz	0
9	1
18	2
37	3
73	4
146	5
293	6
586	7
1172	8
2344	9
4687	10
9375 Hz	11
18.75	12
37.5	13
75	14
150	15
300	16
600 KHz	17
1.2	18
2.4	19
4.8	20
9.6 MHz	21

B — PHASE SIGNIFICANCE

π $\frac{\pi}{2}$ $\frac{\pi}{4}$ $\frac{\pi}{8}$ — — — —

0 0 0 0 1 0 0 0 0 1 1 0 0 1 1 0 0

$W_0 = +620.625$ KHz

C — FREQUENCY DEVIATION ΔW 16-BIT 2'S COMPLIMENT VALUE BETWEEN ∓ 150 KHz

S S S S S S 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

SIGN

SIGN EXTEND

D — BETA $\left(=\frac{1}{1024}\right)$ OF PHASE VALUE TO UPDATE ΔW

S S S S 21 20 19 18 17 16 15 14 13 12 11 10

SIGN

SIGN EXTEND

E — ALPHA $\left(=\frac{1}{4}\right)$ OF PHASE VALUE TO BE SUBTRACTED ONCE PER INPUT TRANSITION FROM THE PHASE ACCUMULATOR
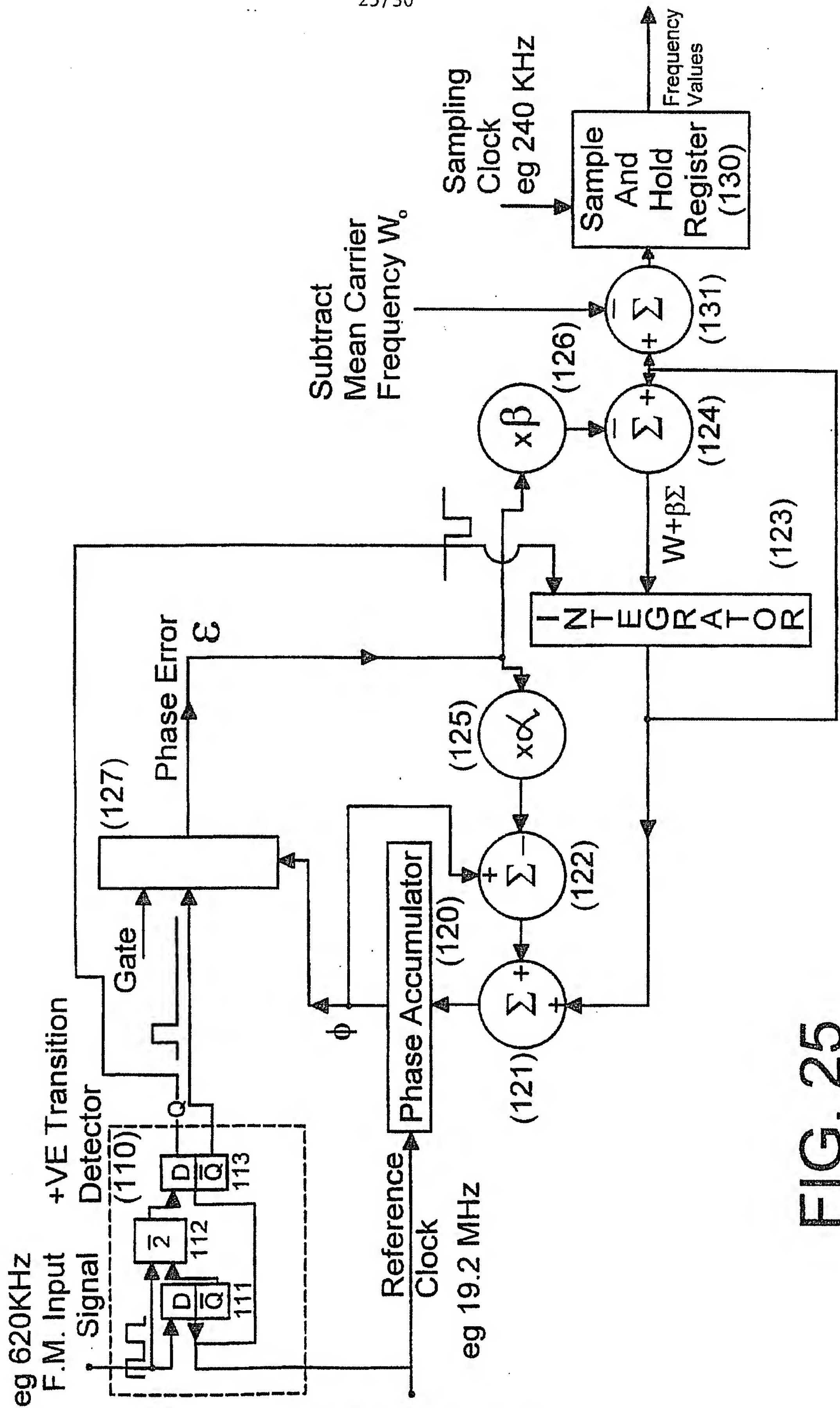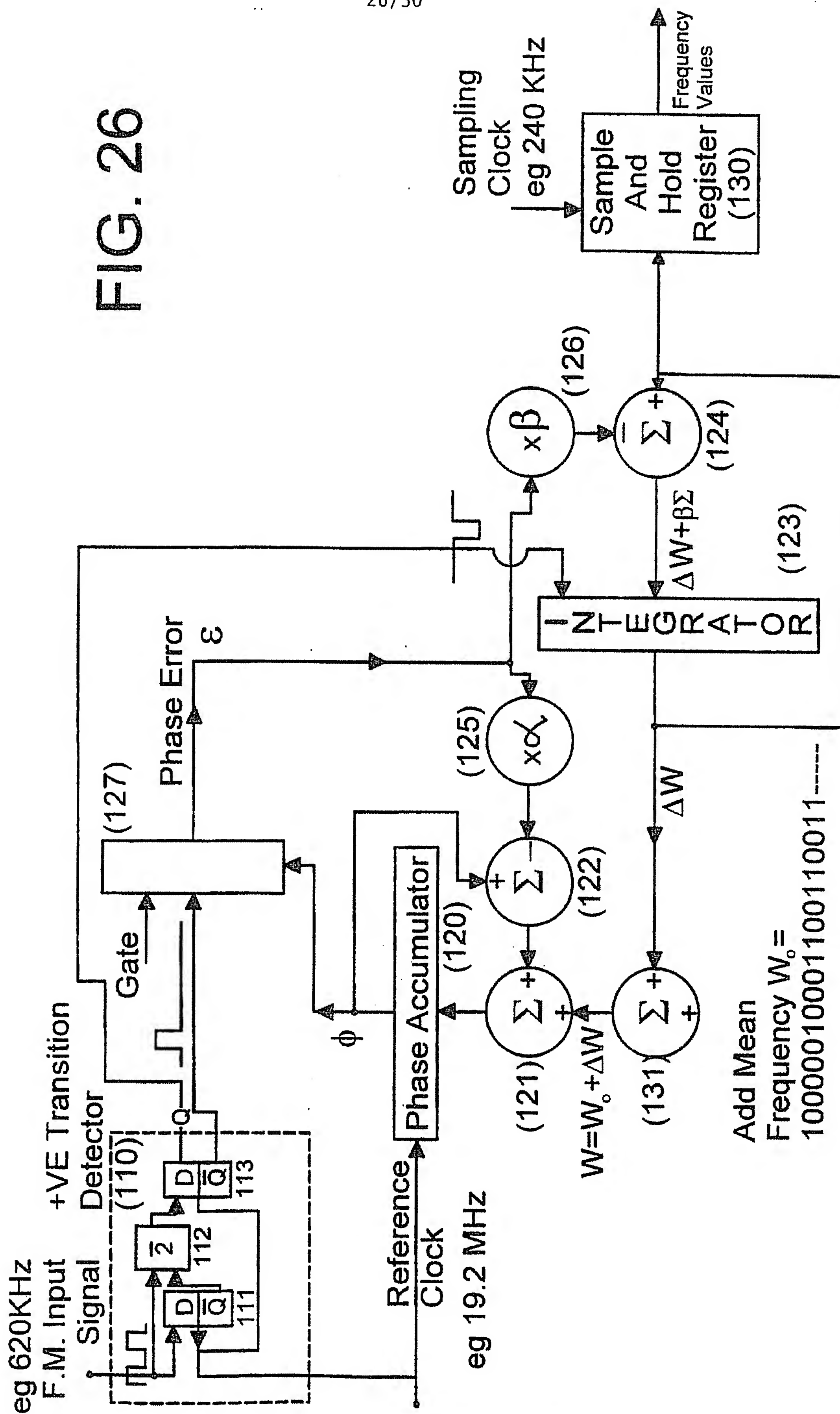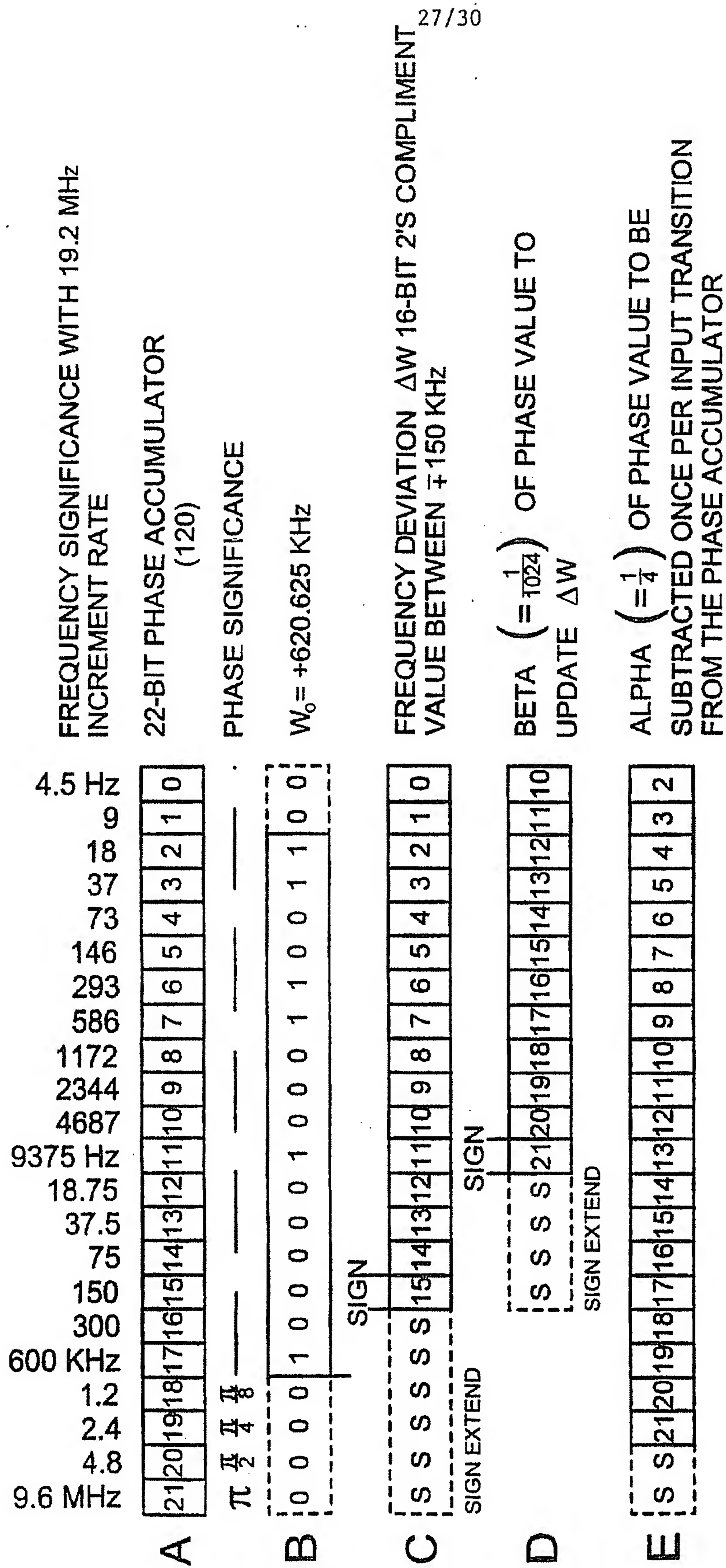
S S 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2

FIG. 27

FIG. 28(b)

FIG. 28(a)
PRIOR ART

FIG. 29

30/30

FIG. 30

INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6   H03M1/60

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6   H03M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GB 2 270 596 A (ARKAS EVANGELOS ;ARKAS NICHOLAS (GB)) 16 March 1994 see page 3, lines 9-29; page 4, lines 4-30; page 5, lines 17-19; figures 1,3 -----	1,17

| | Further documents are listed in the continuation of box C. | X | Patent family members are listed in annex. |

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
24 October 1997	06.11.97

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Beindorff, W

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

Interna   al Application No
PCT/US 97/09038

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
GB 2270596 A	16-03-94	CA	2148273 A	31-03-94
		WO	9407310 A	31-03-94
		EP	0665999 A	09-08-95
		US	5424735 A	13-06-95